

1 15. The integrated circuit of claim 14 including an
2 inverter that creates a high signal in response to a low
3 signal on said feedback path.

1 16. The integrated circuit of claim 15 including a
2 pair of transistors that must both conduct in order to
3 generate said pulses.

1 17. The integrated circuit of claim 16 including a
2 capacitor circuit to enable the supply voltage to reach a
3 designated output level.

1 18. The integrated circuit of claim 17 including a
2 hysteresis sense stage coupled to said capacitor circuit.

1 19. The integrated circuit of claim 11 wherein said
2 activation circuit includes an inverter coupled to the gate
3 of a load transistor, a second transistor coupled to said
4 load transistor and a third transistor coupled between said
5 load transistor and said first transistor.

1 20. The integrated circuit of claim 11 including a
2 circuit to latch the pulse generator in response to the
3 supply voltage being in a first state.

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1 21. A power-on reset pulse generator comprising:
2 a first circuit to develop a pulse indicating
3 that a power supply voltage is not in a first state; and
4 a second circuit coupled to said first circuit to
5 latch the first circuit in response to the power supply
6 voltage being in the first state..

1 22. The generator of claim 21 wherein said second
2 circuit latches the first circuit until the next power
3 cycle.

1 23. The generator of claim 21 including a logic
2 functionality that emulates logic that is difficult to
3 trigger.

1 24. The generator of claim 23 wherein said logic
2 functionality is coupled to the supply voltage.

1 25. The generator of claim 21 wherein said second
2 circuit includes a level detector that detects when a
3 voltage is above at least two transistor threshold
4 voltages, said level detector operative to control said
5 first circuit.

1 26. The generator of claim 21 including a feedback
2 path from the output of said first circuit to said second
3 circuit.

1 27. The generator of claim 26 including an inverter
2 coupled in said feedback path.

1 28. The generator of claim 27 including a pair of
2 transistors that must both conduct in order to generate
3 said pulse.

1 29. The generator of claim 28 including a capacitor
2 circuit to enable the supply voltage to reach a designated
3 output level.

1 30. The generator of claim 29 including a hysteresis
2 sense stage coupled to said capacitor circuit.